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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,406	10/29/2003	Russell W. Guenthner	52003218	7204

7590 12/13/2005

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,406	GUENTHNER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/697,406 filed on 9/28/2005. Claims 1-4 remain pending in the application.

Claim Objections

2. Claims 1 and 3 are objected to because of the following informalities: claim 1, line 1, "the timing performance" should be changed to --a timing performance--; line 4, "the timing of logic signals" should be changed to --timing of logic signals--; line 9, "the logic" should be changed to --logic--; line 16, "the critical logic" should be changed –a critical logic--; "other logic" should be changed to –other logic loads--; line 22, "the selection" and "the placement" should changed to --a selection-- and --a placement--, respectively. Claim 3 has similar pattern. Thus, the objection of claim 3 is likewise the same as in claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being obvious over Rahut et al. (6,766,504) in view of Chen et al. (5,835,751).

5. As to claim 1, Rahut et al. teach a method for optimizing the timing performance of an overall logic circuit implemented in a FPGA (see col. 1) with programmable interconnect behaving in a way that timing of logic signals routed by the programmable interconnect from a specific source to a specific load with the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal (Fig. 1 shown part of the circuit implemented; Fig. 2-3 shown the method for optimizing the timing) comprising a) synthesizing the overall logic for the first implementation in an FPGA including construction and first placement of the logic functions on the FPGA (Fig. 1); b) analyzing the timing (timing information; routing in delay mode; col. 4 lines 23-37); c) determining the most critical timing paths (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37; Fig. 1A-1C, thick line of connections are example of most critical path, disregarding non-critical thin line connections); d) selecting as an object for implementing a specific critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signal contributing to that chosen critical path (at least the reference teaches routing only one more critical connections of a selected logic level

until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information). Rahut et al. do not teach the change being a change in selecting logic elements and placement of those elements. Chen et al. teach identifying clock paths (Fig. 5, items 501-503) including critical paths (col. 14 lines 31-47) by a clock analysis (Fig. 4, item 402). Chen et al. teach, not only to minimize interchip connections (meaning minimizing interconnected routing distance of the signals contributing to a chosen critical path as recited in the claim), and thereby increase utilization of the logic resources of the FPGAs, a duplicate module 408 (Fig. 4) replicates logic element(s) (Fig. 17A, logic 1705 or known as a common logic to critical paths to different loads 1703 and 1704) on the critical path also to minimizing data path delays by avoiding interchip interconnections (col. 15, lines 58-67, col. 16 lines 1-11; col. 16 lines 41-58). With such motivation and expected results, practitioners in the art at the time the invention was made would have found obvious to change logic elements on the critical path as taught by Rahut et al. by selecting logic elements on the critical path and replicate them and then performing routing process in order to minimizing interchip connections and also minimizing data path delays as expected.

6. As to claims 2 and 4, Rahut et al. also teach the implementation of the critical logic in a new way in step e) is limited only to changes in the placement of the logic in the chosen critical path (routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information). In

addition, Chen et al. teach only change in the placement of the logic elements in the chosen critical path (duplication of logic element 1705 in Fig. 17A in order to minimizing interchip connections and also minimizing data path delays (col. 16 lines 41-58).

7. As to claim 3, Rahut et al. teach a method for optimizing the timing performance of an overall logic circuit implemented in a FPGA (see col. 1) with programmable interconnect behaving in a way that timing of logic signals routed by the programmable interconnect from a specific source to a specific load with the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal (Fig. 1 shown part of the circuit implemented; Fig. 2-3 shown the method for optimizing the timing) comprising a) synthesizing the overall logic for the first implementation in an FPGA including construction and first placement of the logic functions on the FPGA (Fig. 1); b) analyzing the timing (timing information; routing in delay mode; col. 4 lines 23-37); c) determining the most critical timing paths (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37; Fig. 1A-1C, thick line of connections are example of most critical path, disregarding non-critical thin line connections); d) selecting as an object for implementing a specific critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of

logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signal contributing to that chosen critical path (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37); f) modifying the placement of other logic in the overall logic circuit in accommodate the changes in placement of the chosen critical path while maintaining approximately the new placement of the critical logic and g) repeating the step b) through f) where the last implementation and placement of the overall logic circuit from step f) becomes the basis for starting again with this last implementation becoming the base implementation (at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads; col. 4, lines 23-37) (see also summary, Fig. 1-3 and its description for detailed information).). Rahut et al. do not teach the change being a change in selecting logic elements and placement of those elements. Chen et al. teach identifying clock paths (Fig. 5, items 501-503) including critical paths (col. 14 lines 31-47) by a clock analysis (Fig. 4, item 402). Chen et al. teach, not only to minimize interchip connections (meaning minimizing interconnected routing distance of the signals contributing to a chosen critical path as recited in the claim), and thereby increase utilization of the logic resources of the FPGAs, a duplicate module 408 (Fig. 4) replicates logic element(s) (Fig. 17A, logic 1705 or known as a common logic to critical paths to different loads 1703 and 1704) on the critical path also to minimizing data path delays by avoiding interchip interconnections (col. 15, lines 58-67, col. 16 lines 1-11;

col. 16 lines 41-58). With such motivation and expected results, practitioners in the art at the time the invention was made would have found obvious to change logic elements on the critical path as taught by Rahut et al. by selecting logic elements on the critical path and replicate them and then performing routing process in order to minimizing interchip connections and also minimizing data path delays as expected.

Remarks

8. Examiner appreciates explanation by Mr. Russell Goethe (54,140) on 12/2/05 regarding to step e) in claim 1. As in the remarks filed with the amendment on 9/28/05, step e) in claim 1, has been clarified that the change of selected logic elements has been made by duplicating the logic elements and placement of duplicated logic elements for routing to minimize interconnection. These claimed limitations have found in Chen et al. patent as described in above rejection. Therefore, the present claims are not patentable over the combination of the cited references.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER